REMARKS

The Office Action dated July 12, 2007 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1-4, 7-13, 17-24, 26-31 and 32-33 have been amended to more particularly point out and distinctly claim the subject matter which is the invention. Claims 34-36 have been added. Claims 6, 16 and 27 have been cancelled without prejudice or disclaimer. No new matter has been added. Claims 1-5, 7-8, 11-15, 17-18, 21-26, 28-29, and 32-36 are submitted for consideration.

Claim 2 was objected to because of informalities. Claim 2 has been amended to overcome the objection. Therefore, Applicant requests that the objection be withdrawn.

Claims 8-10, 18-20 and 29-31 were indicated to be allowable and were objected to as being based on a rejected base claim. Some of the features of claims 6, 9-10, 16, 19-20, 27 and 30-31 have been incorporated into independent claims 1, 11, 26 and 33. Therefore, Applicant requests that each of claims 1, 11, 26 and 33, and the dependent claims thereon, also be allowed and that the rejection of the claims 1, 11, 26 and 33, and the dependent claims thereon, be withdrawn.

Claims 1-4, 6, 11-14, 16, 21-24, 26, 27, 32 and 33 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,790,608 to Benayoun (hereinafter Benayoun). The rejection is traversed as being based on a reference that does not teach

or suggest each of the elements of claims 1-4, 6, 11-14, 16, 21-24, 26, 27, 32 and 33, and newly added claims 34-36.

Claim 1, upon which claims 2-10 depend, recites a method for synchronizing a receiver to a transmitter. The method includes receiving, by the receiver, a phase difference information indicating a phase difference between an internal clock and an external clock and generating, by the receiver, a clock signal dependent on the transmitted phase difference information. The method also includes generating, by the receiver, an internal clock or recovering an internal clock of the transmitter from information received from the transmitter and frequency-dividing, by the receiver, the internal clock. The method further includes adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information and storing, by the receiver, at least two successive values of the phase difference information received from the transmitter. The method also includes detecting, by the receiver, a difference between the successive values of phase difference information.

Claim 11, upon which claims 12-20 depend, recites a system for synchronizing a receiver to a transmitter. The system includes a transmitter including a phase difference information generating unit configured to generate phase difference information indicating a phase difference between an internal clock and an external clock, and a transmitting unit configured to transmit the phase difference information to the receiver. The system also includes a receiver including a receiving unit for receiving a phase difference information indicating a phase difference between an internal clock and an

external clock and a clock generator unit configured to generate a clock signal dependent on the transmitted phase difference information. The receiver also includes a generating unit configured to generate an internal clock or recover the internal clock of the transmitter from information received from the transmitter, a frequency-dividing unit configured to frequency-divide the internal clock. The receiver also includes an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information, a storing unit configured to store at least two successive values of the phase difference information received from the transmitter, and a detecting unit configured to detect a difference between the successive values of phase difference information.

Claim 21, upon which claims 22-25 depend, recites a transmitter used in a system for synchronizing a transmitter and a receiver, wherein the receiver includes a clock generator means for generating a clock signal dependent on the transmitted phase difference information. The transmitter includes a plurality of dividers wherein an external synchronization input is applied to one of the plurality of dividers which is configured to generate an external timebase and a symbol clock from an internal clock is applied to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. The transmitter also includes a phase difference generating unit configured to generate phase difference information indicating a phase difference between an internal clock and an external clock. The internal timebase and the external timebase are applied to start and stop input

of the phase difference generating unit. The transmitter further includes a symbol generator to which the phase difference is applied, the symbol generator is also configured to receive a symbol clock generated by an internal clock generator and a transmitting unit configured to transmit the phase difference information to a receiver.

Claim 26, upon which claims 27-31 depends recites a receiver used in a system for synchronizing a receiver to a transmitter. The transmitter includes a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver. The receiver includes a receiving unit configured to receive a phase difference information indicating a phase difference between an internal clock and an external clock and a clock generator unit configured to generate a clock signal dependent on a phase difference information transmitted from a transmitter. The receiver also includes a generating unit configured to generate an internal clock, or to recover the internal clock of the transmitter from information received from the transmitter. The receiver further includes a frequency-dividing unit configured to frequency-divide the internal clock and an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information. The receiver also includes storages for storing at least two successive values of the phase difference information received from the transmitter and a detector unit configured to detect a difference between the successive values of the phase difference information.

Claim 32 recites a method for synchronizing a transmitter and a receiver wherein the receiver generates a clock signal dependent on a transmitted phase difference information. The method includes applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an internal clock to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. The method also includes generating, by a transmitter, phase difference information indicating a phase difference between an internal clock and an external clock. The internal timebase and the external timebase are applied to start and stop input of the phase difference generating unit. The method further includes applying the phase difference to a symbol generator, the symbol generator is also configured to receive a symbol clock generated by an internal clock generator and transmitting, by the transmitter, the phase difference information to the receiver.

Claim 33 recites a method for synchronizing a receiver to a transmitter. The transmitter generates phase difference information indicating a phase difference between an internal clock and an external clock. The method includes receiving, by the receiver, a phase difference information indicating a phase difference between an internal clock and an external clock and generating, by the receiver, a clock signal dependent on a transmitted phase difference information indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter. The method also includes generating, by the receiver, an

internal clock or recovering the internal clock of the transmitter from information received from the transmitter and frequency-dividing, by the receiver, the internal clock. The method further includes adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information and storing, by the receiver, at least two successive values of the phase difference information received from the transmitter. The method also includes detecting, by the receiver, a difference between the successive values of phase difference information.

As outlined below, Benayoun does not teach or suggest each of the elements of claims 1-4, 6, 11-14, 16, 21-24, 26, 27, 32 and 33.

Benayoun discloses a method for synchronizing the clock signal of a first data terminal equipments to a second data terminal equipment connected to a communication network through a first network node and a second network node. The communication network has a reference clock that it transmits to the second network node which compares it with the clock signal it receives from the second data terminal equipment. The phase difference is then detected and converted into a frame which may be an ATM cell or any other frame so that it can be switched with the data frames sent to the second data terminal equipment and transmitted to the first data terminal equipment.

Applicant submits that Benayoun does not teach or suggest each of the elements of claims 1-4, 6, 11-14, 16, 21-24, 26, 27, 32 and 33. Each of claims 21 and 33, in part, recites applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an

internal clock to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. Benayoun does not each or suggest these features.

There is no disclosure in Benayoun of one a plurality of dividers to which an external synchronization input is applied and which is configured to generate an external timebase. There is also no teaching or suggest in Benayoun of another one of the plurality of dividers to which a symbol clock from an internal clock is applied and which is configured to generate an internal timebase of the same frequency as the external timebase.

Each of independent claims 1, 11, 26 and 32, in part, recites storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting, by the receiver, a difference between the successive values of phase difference information. Benayoun does not each or suggest these features.

The Office Action noted that claims 9 and 10 are allowable. Claims 9 and 10 previously recited storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting, by the receiver, a difference between the successive values of phase difference information. These allowable features are now recited in claims 1, 11, 26 and 32. There is no disclosure in Benayoun of storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting, by the receiver, a difference between the successive values of phase difference information. Therefore,

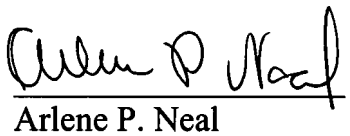
Applicant requests that the rejection under 35 U.S.C. 102(b) be withdrawn because Benayoun does not teach or suggest each of the elements of claims 1, 11, 21, 26, 32 and 33, and hence dependent claims 1-10, 12-20, 22-25 and 27-21 thereon.

According, Applicant submits that claims 1-5, 7-8, 11-15, 17-18, 21-26, 28-29, and 32-36 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 1-5, 7-8, 11-15, 17-18, 21-26, 28-29, and 32-36 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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Enclosures: Additional Claim Fee Transmittal
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